Western CubeSat Project

Solar panel info and assembly

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# Overview

The purpose of this document is to provide info regarding the equipment required, overall design, and assembly instructions of Western University’s CubeSat’s solar panels.

The solar panels play a vital role in several subsystems of the CubeSat:

* Deliver power to the CubeSat.
* Return sensor data from photodiodes and temperature sensors for attitude determination.
* Control and sense the deployment of the communication antennas.
* Removable RBF pin that will keep the CubeSat deactivated.
* Offers a bypass to the OCB and EPS components USB ports.
* Access to the jumper pins of the EPS for testing purposes.
* Connectors to access internal accelerometers for vibration tests.

# Parts requiring additional work

The design of the listed components should be completed before attempting to assemble solar panels:

* ±Z end-plate PCBs for mounting sensors and rad-hardened voltage reference.
* A proper antenna release mount with burn-wire.
* Determination of number of internal accelerometers for vibration testing, and the wiring requirements of them.

# Assumptions

Several assumptions have been made in this document:

* All components have been tested and assured that they work.
* The solar cells have been electrically tested and confirmed they are working according to the specifications given in [6].
* The additional components (antenna release mount, photodiode mounts) have been created and properly assembled.
* A PCB has been created according to the required PCB design specifications (see section 8).
* Knowledge of CSA standards for assembly of components.
* Ability to solder small components with accuracy.
* Assembly is being performed in cleanroom of minimum class 100,000.

# Required equipment

* NuSil CV4-1161-5 Adhesive Tape (double-sided)
* Silver foil contact (for additional connectors)
* Epoxy Technology - EPO-TEK® H20E silver epoxy
* Kapton tape for general use
* Adhesive bonding/clear staking
* Vacuum tweezers for handling
* Solder
* Soldering iron
* Solvent and flux remover
* Compressed air
* Laboratory grade isopropyl alcohol
* Scissors
* Sharp Exacto knife
* Aluminum solar cell template for NuSil cutouts
* Credit-card type material to apply pressure when laying solar cells
* Rubber gloves
* Safety glasses
* Visual magnification

# Panel variants

There are three variants of the solar panels. Each variant shares common components, but also has its own specific components depending on which face of the CubeSat it is (e.g. the panel with the RBF switch must be on the +Y face as that is the face of the access door of the NanoRacks pod).

Components that are common to all of the panels are:

* Photodiode mount and photodiodes
* Antenna release mount and sensor
* Temperature sensor
* ADC and Op-amps
* Solar cells

Terms related to the building of the panels:

* **Bottom-side** - refers to the face of the panel that is against the CubeSat rails.
* **Top-side** - refers to the face of the panel away from the rails, and has the solar cells mounted on it.
* **PCB** – printed circuit board.
* **EPS** – the CubeSat’s electrical power system.
* **OBC** – the CubeSat’s onboard computer.
* **JTAG** – the programming interface for the OBC.
* **RBF** – remove before flight switch and pin
* **ADC** – analog-to-digital converter.
* **USB** – connector type used to interface with the EPS and OBC.

## 5.1. RBF, EPS jumper wires, EPS bypass panel (+Y face)

This panel contains the RBF switch, jumper wires for the EPS JMP1 and JMP2, and a USB bypass to the EPS USB connector. The JMP1 and JMP2 pins are used to disable the self-locking functionality of the EPS, and to allow charging of the batteries via the USB EPS bypass. The EPS bypass also allows for monitoring and control of the EPS.

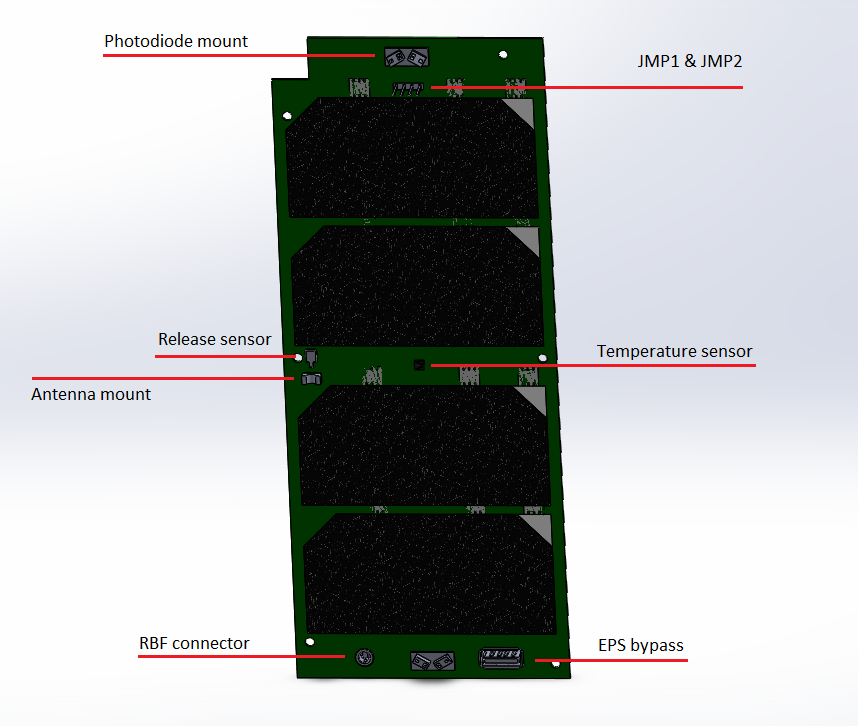


Figure 1, RBF/EPS panel top-side

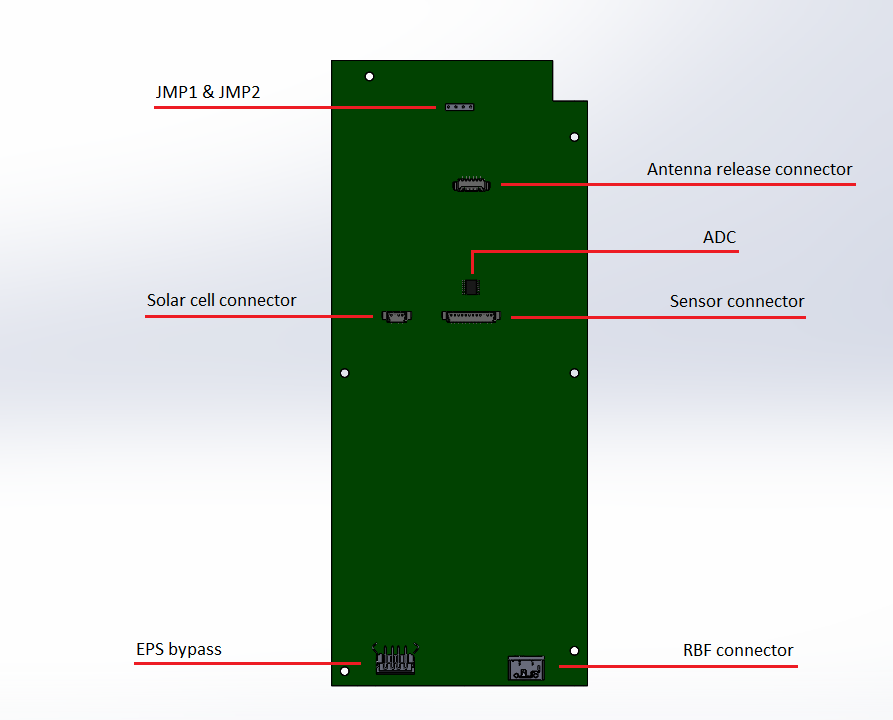


Figure 2, RBF/EPS panel bottom-side

## 5.2. JTAG and OBC bypass panel (-X face)

This panel contains the JTAG and OBC bypasses. The JTAG pins of the OBC are used to program it, and this panel allows access to those internal pins when the solar panels are attached. The OBC bypass provides access to the OBC’s USB port so that an external device (e.g. laptop) may be connected to it.

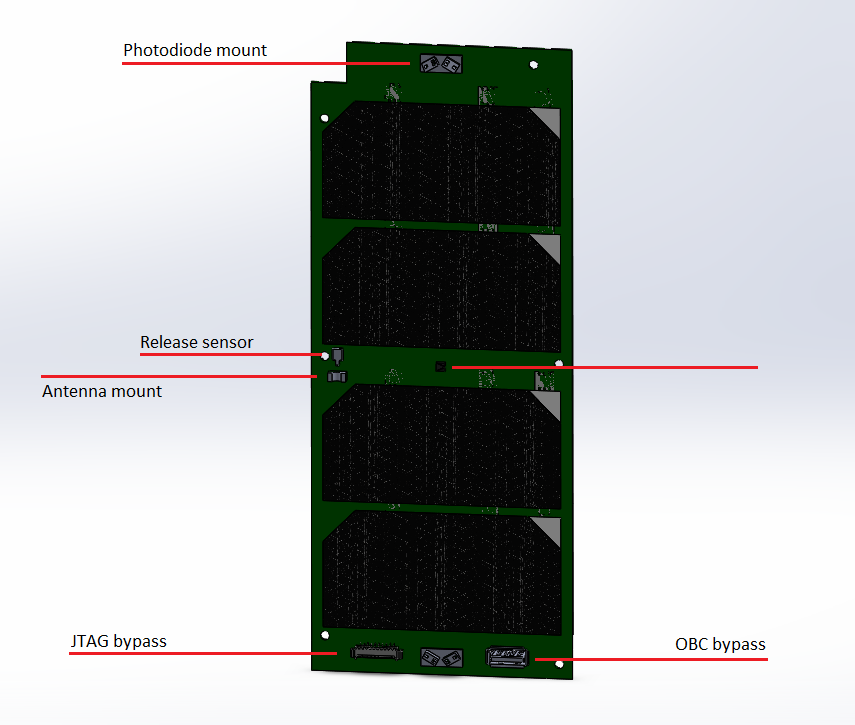


Figure 3, JTAG/OBC panel top-side

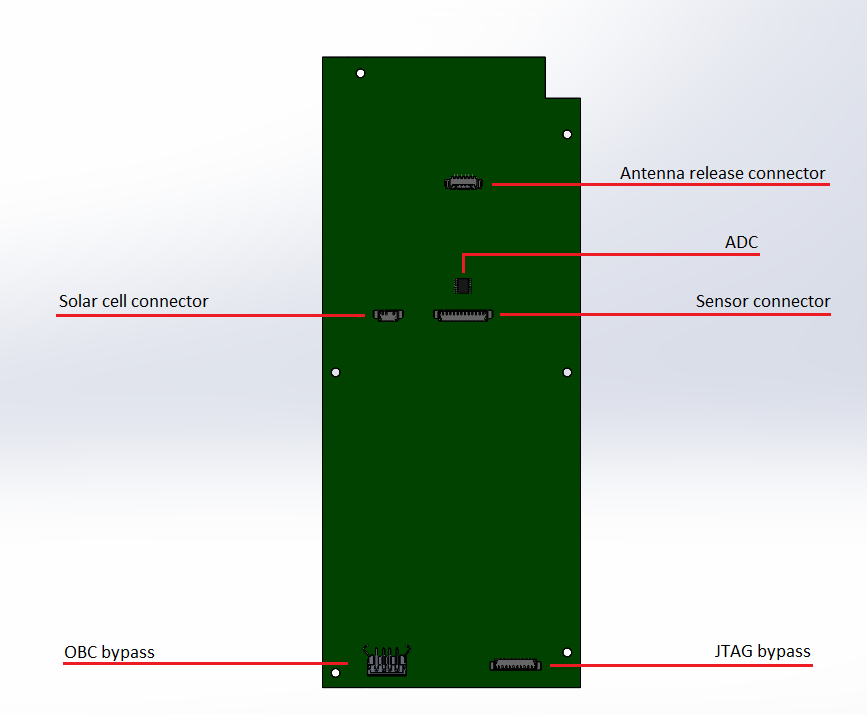


Figure 4, JTAG/OBC panel bottom-side

## 5.3. Accelerometer (+X, -Y faces)

These panels provides access to internal accelerometers used for vibration testing. Connectors are placed on both the top-side and bottom-side of the panel and are connected together. Accelerometers may be connected to the bottom-side connectors, and a device to the top-side ones. Once vibration testing is complete, the external cables may simply be disconnected and the internal ones left alone. A number of connector pairs are only needed for however many accelerometers are required, and thus the connectors are optional if they will not be used.

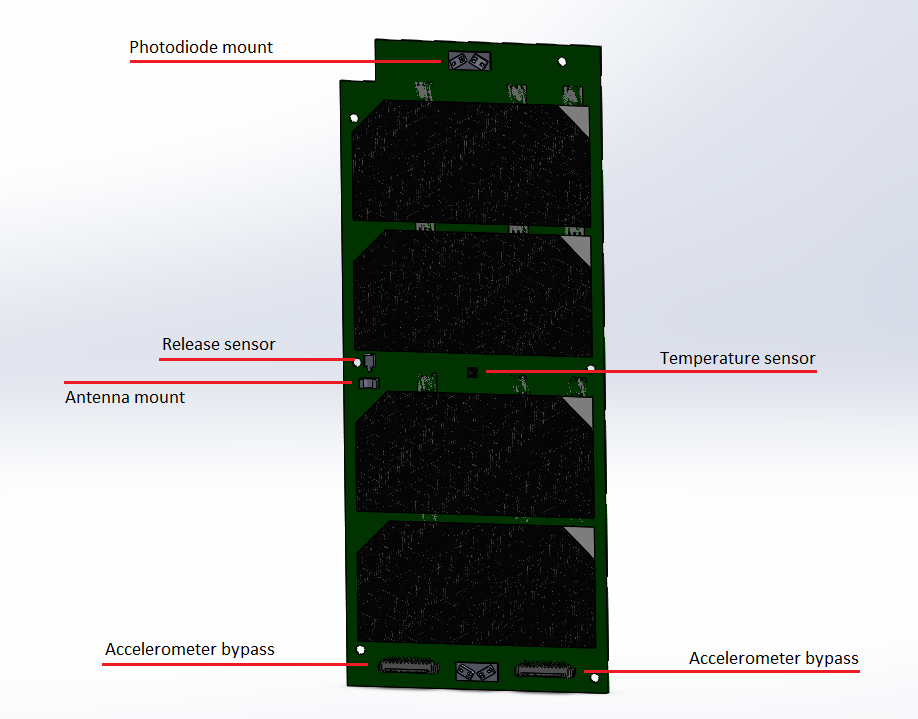


Figure 5, Accelerometer panel top-side

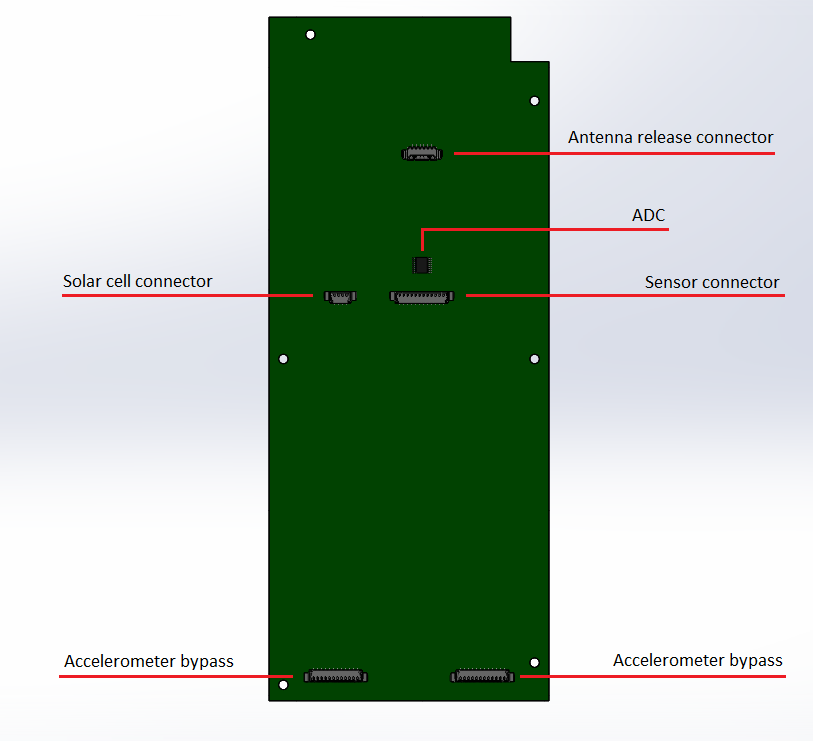


Figure 6, Accelerometer panel bottom-side

## 5.4. End-plates (+Z, -Z)

Currently there is no set physical design for these plates, however they will be relatively simple compared to the other variants in that they will not hold any solar cells or provide power to the EPS. The purpose of this variant is to serve as a mounting point for sensors on the ±Z ends.

The sensors contained on these boards will be 3 TEMD6010FX01 photodiodes and their circuits, 1 LM70 temperature sensor, 1 [RH1009 2.5V rad-hardened reference voltage](https://www.analog.com/media/en/technical-documentation/data-sheets/RH1009.pdf), and 1 MAX1249 ADC. The purpose of the rad-hardened 2.5V reference is to provide insight on how much external radiation is shifting the readings produced by the ADC by comparing its current digital output to a radiation-free digital output. This difference may then be applied to all other simultaneous ADC readings to provide more accurate values.

# Required components

The solar panel variants share common components, but also have several components that are unique to them. The quantities of components given are per a single panel, and thus 4 sets of the common components list will be needed for 4 panels.

## 6.1. Common components

|  |  |
| --- | --- |
| Component | Quantity |
| AZUR SPACE 3G30A Solar cells | 4 |
| PCB | 1 |
| Photodiode mounts | 2 |
| TEMD6010FX01 photodiodes | 4 |
| LTC6340HV Op-amp | 4 |
| LT6202 Op-amp | 4 |
| MAX1249 ADC | 1 |
| LM70 Temperature sensor | 1 |
| 570pF capacitor | 4 |
| 11pF capacitor | 4 |
| 0.1μF capacitor | 1 |
| 22.1kΩ resistor | 4 |
| 562Ω resistor | 4 |
| Antenna release mount | 1 |
| TE Connectivity JJDVDUJ314 Antenna release sensor | 1 |
| MOLEX 53398-0471 (Solar cell connector) | 1 |
| MOLEX 53398-1271 (Sensor connector) | 1 |
| MOLEX 53261-0671 (Antenna release connector) | 1 |

Figure 7, common components

## 6.2. RBF/EPS variant unique components

|  |  |
| --- | --- |
| Component | Quantity |
| Pin header (4 pins, JMP1 & JMP2) | 1 |
| MOLEX 67643-2911 (EPS bypass) | 1 |
| MOLEX 47257-0001 (RBF switch connector) | 1 |
| Tensility International Corp 50-00402 | 1 |

Figure 8, RBF/EPS components

## 6.3. JTAG/OBC variant unique components

|  |  |
| --- | --- |
| Component | Quantity |
| MOLEX 67643-2911 (OBC bypass) | 1 |
| MOLEX 53261-1071 (JTAG bypass external) | 1 |
| MOLEX 53398-1071 (JTAG bypass internal) | 1 |

Figure 9, JTAG/OBC components

## 6.4. Accelerometer variant unique components

|  |  |
| --- | --- |
| Component | Quantity |
| MOLEX 53261-1271 (Accelerometer bypass, top-side) | 2 |
| MOLEX 53398-1271 (Accelerometer bypass, bottom-side) | 2 |
| Accelerometers | ? |

Figure 10, Accelerometer components

## 6.5. End-plates unique components

|  |  |
| --- | --- |
| Component | Quantity |
| Analog Devices RH1009 Radiation Hardened 2.5V Reference | 1 |

Figure 11, End-plates components

# Electrical and sensor design

There are several distinct circuits included in the solar panel assembly. They are mainly to provide power, sensor data, or bypasses to internal components for easier testing. The exact pin connections for the MOLEX connectors can be found in the specifications document [6].

## 7.1. Solar cells (±X, ±Y faces)

[AZUR SPACE’s 3G30A](http://www.azurspace.com/images/products/0003805-01-01_DB_3G30A.pdf) solar cell assemblies were selected to be used for the solar panels. The solar panel circuit contains a total of 4 solar cells: 2 parallel strings of 2 cells in series as shown in the following figure:

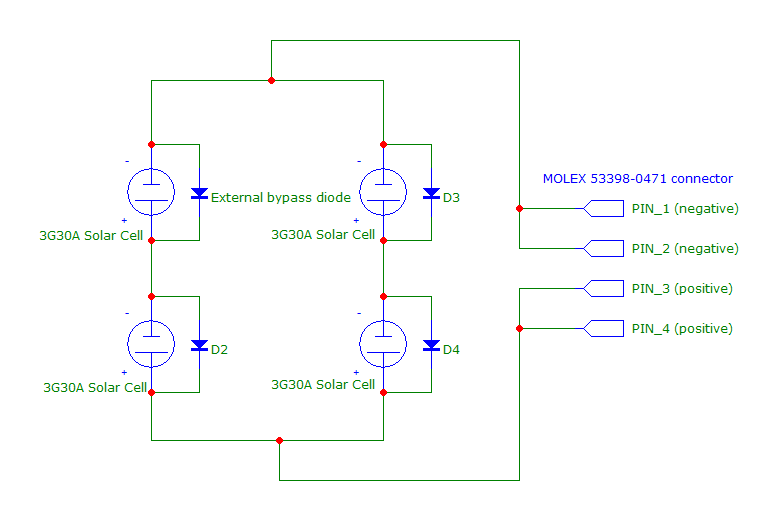


Figure 12, solar cell circuit

The 3G30A solar cell’s connection scheme is as follows. The two top-side connectors are the negative terminals of the cell, while the entire bottom-side plate is the positive terminal. The solar cell also comes with an attached silicon bypass diode with its cathode connected to the bottom-side positive terminal of the cell, and its anode left free for connection (may connect to the negative terminals). This bypass diode prevents the entire output of a string of solar cells from being inhibited when a shadow is cast upon one of the cells. The terminals are as shown in the figure:

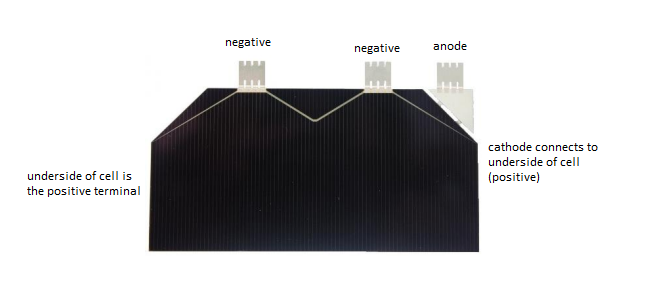


Figure 13, 3G30A connection scheme

On the backside of the solar panel, the [MOLEX 53398-0471](https://www.molex.com/molex/products/datasheet.jsp?part=active/0533980471_PCB_HEADERS.xml) connector is used. This connector provides 4 pins, 2 for positive and 2 for negative in order to provide redundancy. Refer to the specifications given in [6] for the exact pin connections.

## 7.2. Sensors (±X, ±Y faces)

The sensors circuits consist of photodiodes, an ADC, and a temperature sensor (and a rad-hardened voltage reference on the +-Z end plates).

The photodiodes used are [Vishay’s TEMD6010FX01](https://www.vishay.com/docs/81308/temd6010.pdf), and each has their output current modified to a voltage range (0V to 3.3V) readable by the ADC through use of op-amps ([LTC6240HV](https://www.analog.com/media/en/technical-documentation/data-sheets/624012fe.pdf) and [LT6202](https://www.analog.com/media/en/technical-documentation/data-sheets/620234fd.pdf)) as shown:

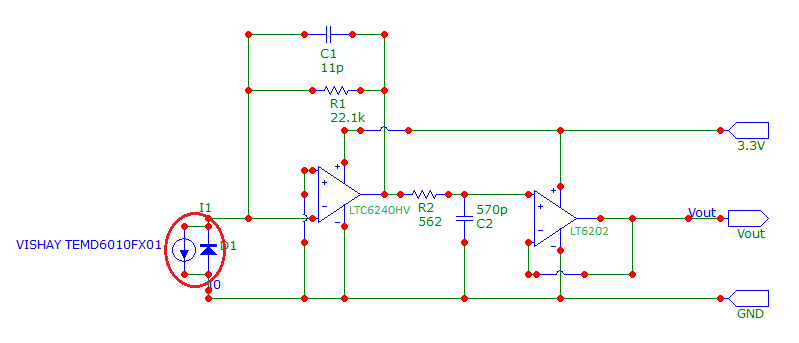


Figure 14, photodiode circuit

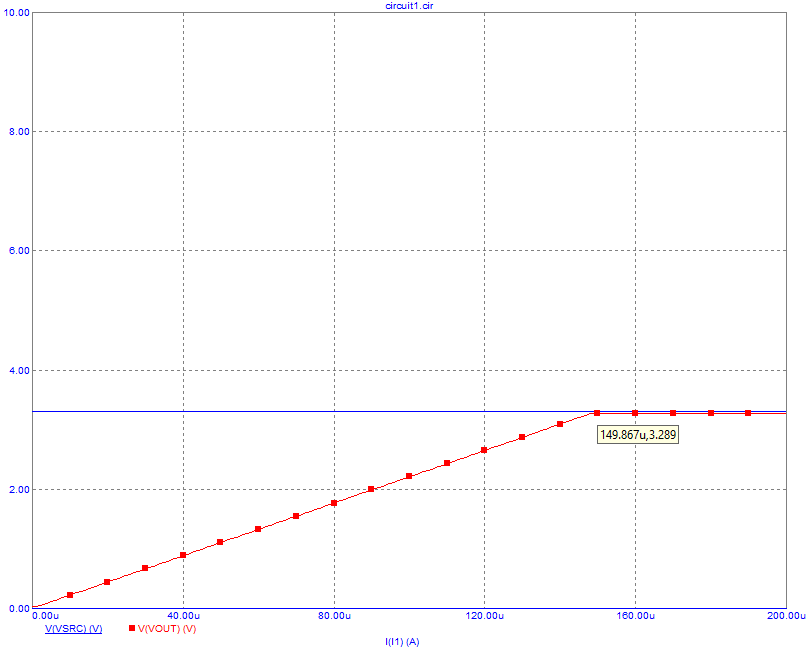


Figure 15, photodiode circuit: current vs. Vout

The photodiodes are to be mounted on the angled photodiode mounts at the top and bottom of the solar panel.

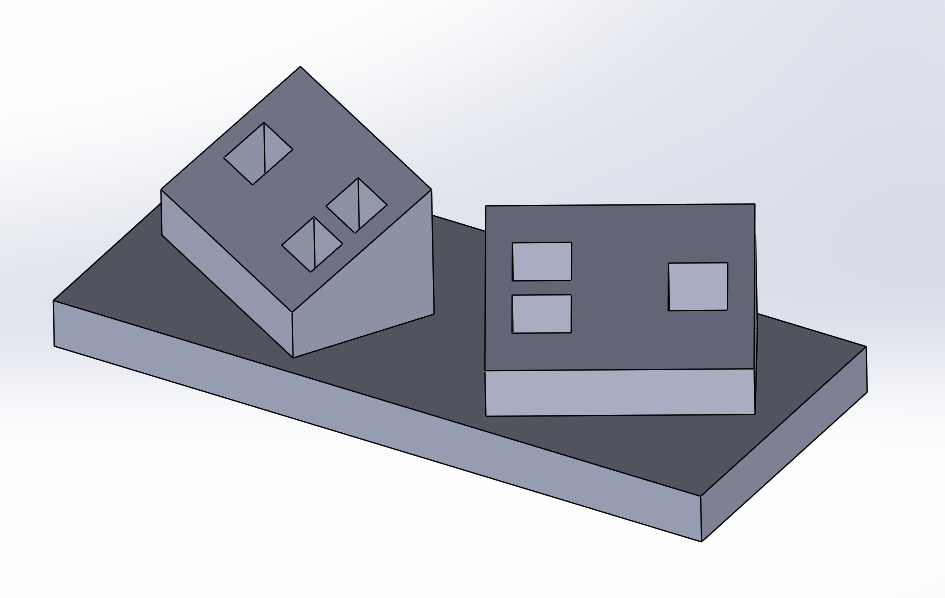


Figure 16, photodiode mount

The photodiodes resultant facing vector once mounted should be 30 degrees towards the Z-axis, and rotated 30 degrees about the panel’s normal vector towards the closest X/Y face edge, as show in Figure 18. This configuration was chosen as it gave an optimal photodiode coverage of the area surrounding the CubeSat (along with 3 normal-facing photodiodes on both of the ±Z end plates).

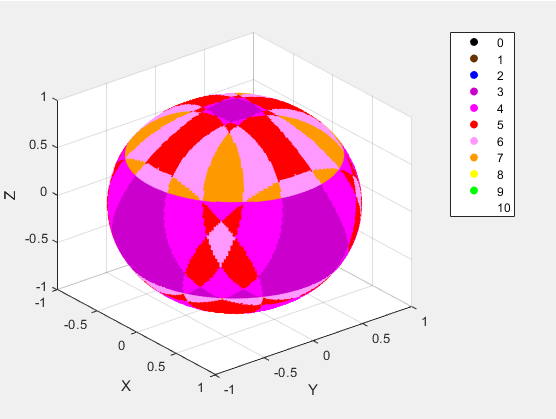


Figure 17, MATLAB simulation, 100% area coverage with >= 3 photodiodes, 70% with >= 4

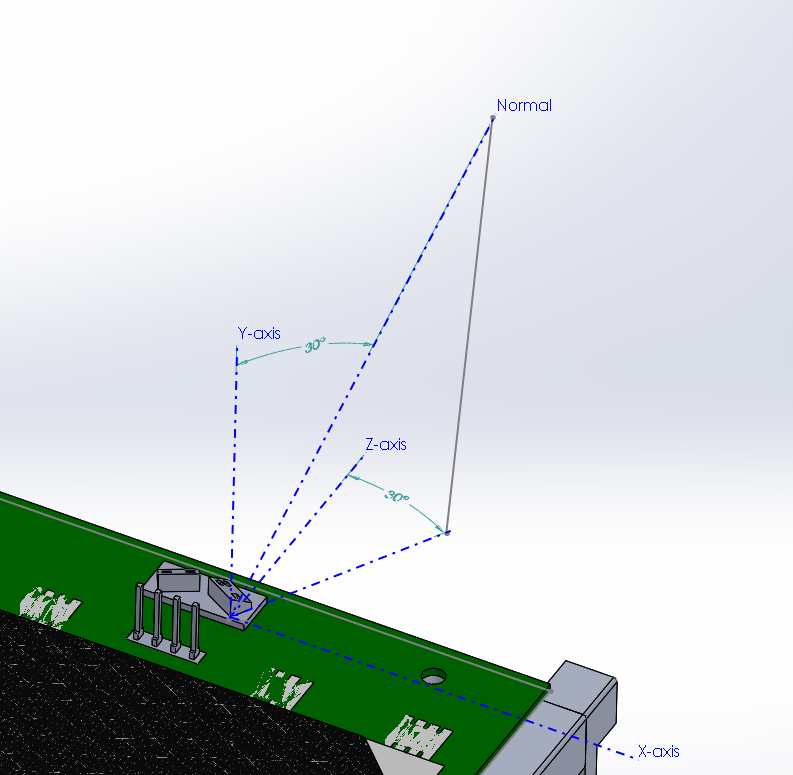


Figure 18, Photodiode mount normal vector angles

The overall circuit consists of [Maxim Integrated’s MAX1249](https://datasheets.maximintegrated.com/en/ds/MAX1248-MAX1249.pdf) ADC, 4 photodiode circuits connected to the ADC’s analog inputs, and 1 [Texas Instruments LM70](http://www.ti.com/lit/ds/symlink/lm70.pdf) temperature sensor. The ADC and temperature sensor are both connected to the SPI interface pins of the [MOLEX 53398-1271](https://www.molex.com/molex/products/datasheet.jsp?part=active/0533981271_PCB_HEADERS.xml) connector.

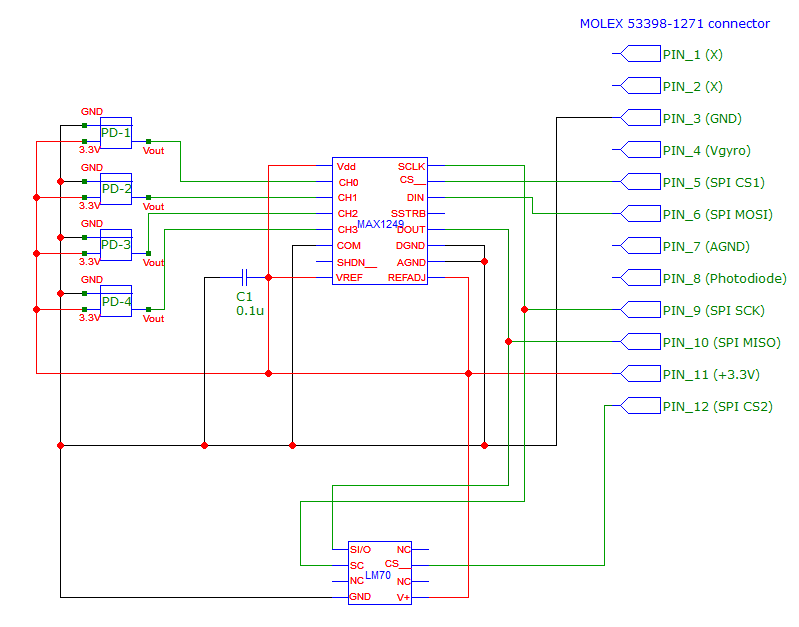


Figure 19, overall circuit

## 7.3. RBF (+Y face)

The RBF circuit utilizes a jack connector, where the circuit is in a closed state when the RBF pin is inserted. When the RBF pin is removed, a circuit on the internal custom board will maintain a ‘closed’ state for 30 minutes through the use of timer components, which will keep the CubeSat turned off until that time is up. This timer may be disabled by use of the EPS JMP pins that disable the self-locking functionality.

A [MOLEX 47257-0001](https://www.digikey.com/product-detail/en/molex/0472570001/WM17366-ND/3262245) jack connector is embedded in the panel, which may be used with a 3.50mm plug. The chosen plug is [Tensility International Corp 50-00402](https://www.digikey.ca/product-detail/en/tensility-international-corp/50-00402/839-1227-ND/4865081). In order to meet the CubeSat design specifications, the RBF pin must extend no more than 6.50mm from the surface of the rails. In order to meet this requirement, the non-connector end of the plug must be shaved down.

The solar panel containing the RBF switch MUST be mounted on the +Y face of the CubeSat. Additionally, the panel must be rotated such that the RBF switch is on the –Z end of the CubeSat in order to be accessible via the NanoRacks access port.

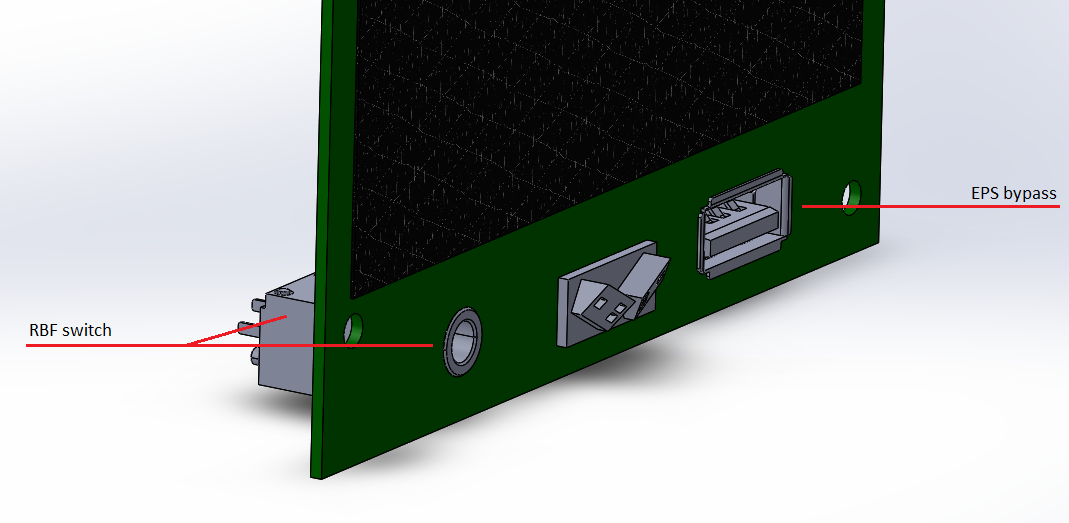


Figure 20, RBF location

## 7.4. OBC/EPS bypass (-X, +Y faces)

The bypass circuit is used to access the USB connectors of both the OBC and EPS for testing purposes. A custom cable will utilize a PC’s USB port and will connect to the exposed connector pins on the solar panel.

This connector will allow for debug of the OBC, and for monitoring, control, and charging of the EPS. A [MOLEX 67643-2911](https://www.digikey.ca/product-detail/en/molex/0676432911/WM4078-ND/2421596) connector is embedded in –Z end of the solar panel, which may be connected to either of the USB1 ports of the OBC or EPS. This connector is only used in the +Y and +X panels.

## 7.5. Accelerometer bypass (+X, -Y faces)

The accelerometer bypass is used to access the internal accelerometers that are used for vibration testing. A [MOLEX 53261-1271](https://www.molex.com/molex/products/datasheet.jsp?part=active/0532611271_PCB_HEADERS.xml) connector (recommended) will be mounted on the top-side surface of the solar panel, which can be connected to so that acceleration measurements maybe made. This requires no cutting of wires, and instead the cable can be simply disconnected before flight. The bottom-side connector is tentatively chosen to be the [MOLEX 53398-1271](https://www.molex.com/molex/products/datasheet.jsp?part=active/0533981271_PCB_HEADERS.xml) connector, however the wiring requirements of the accelerometers is not yet defined.

It is recommended to mount the accelerometer bypasses on either of the –X or +Y faces as the available space on the other faces is already used by the recommended configuration. However this is variable and may be changed as needed.

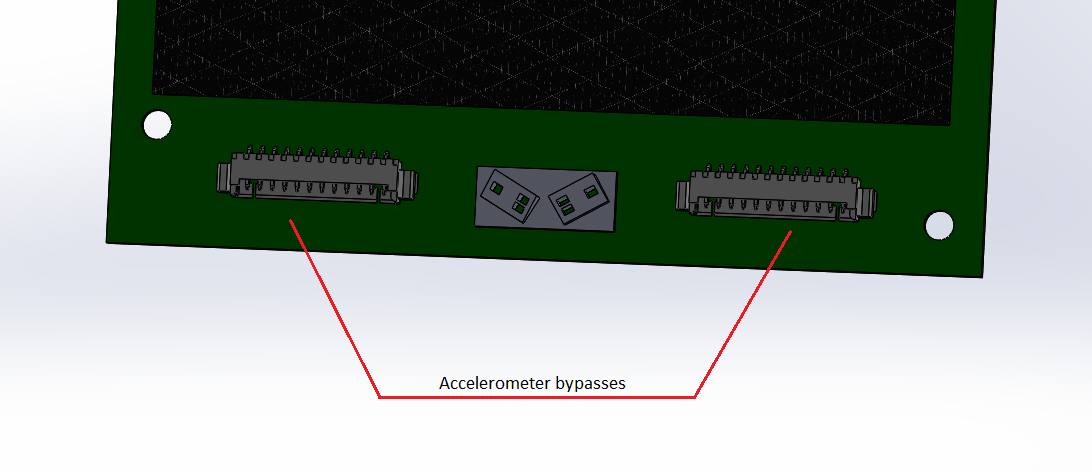


Figure 21, Accelerometer bypass top-side

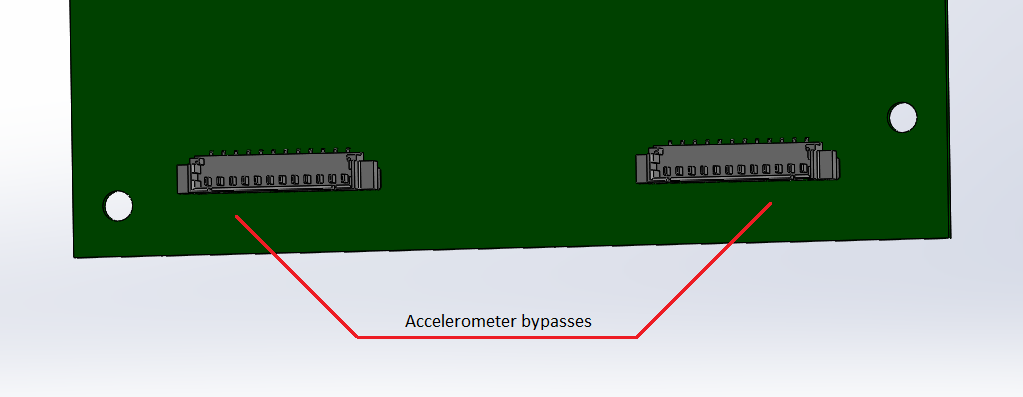


Figure 22, Accelerometer bypass bottom-side

## 7.6. EPS jumper wires (+Y face)

The jumper wires are used to disable the self-locking functionality of the EPS, and to allow charging of the EPS batteries through the EPS bypass. They should also be used to disable the 30-minute timer on the OBC custom board for testing purposes.

The jumper wire pins will be exposed on the outward facing surface of the solar panel. This allows easier access to JMP1 and JMP2 of the Endurosat EPS when the solar panels are attached. The pins may then be cut off before flight. However this connector is optional, and is not required if the EPS is left exposed during testing.

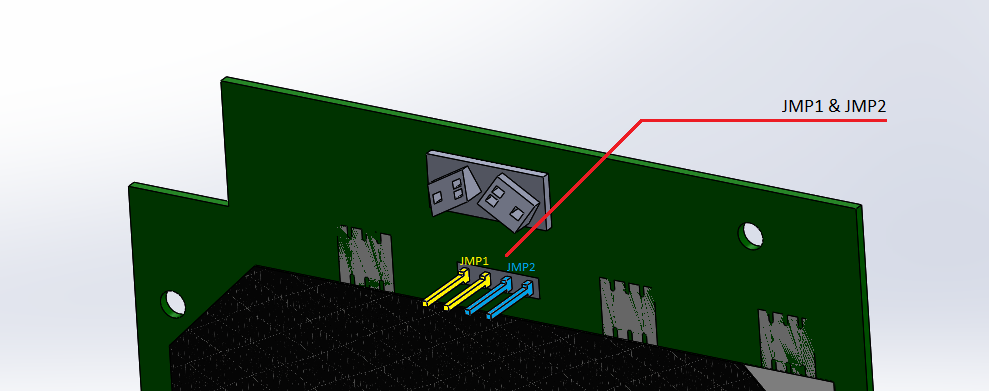


Figure 23, JMP1 & JMP2 pins

## 7.7. Antenna deploy (±X, ±Y faces)

The antenna deploy circuit contains resistors used for burning the burn wire attached to the deploy mount. When the resistors are given a current, they will heat up and break the wire, releasing the antenna.

Additionally, the circuit also contains a switch sensor. When the antenna is released, the switch is in a normally closed state. When the antenna is stowed, the switch is in an open state. This switch is used to detect the deployment of the antennas. The switch is a [TE Connectivity JJDVDUJ314NCPMRTR](https://www.digikey.ca/product-detail/en/te-connectivity-alcoswitch-switches/JJDVDUJ314NCPMRTR/450-3308-1-ND/9452506), which will fit flat against the surface of the top-side of the panel.

## 7.8. Programming interface (-X face)

The programming interface allows a bypass to the JTAG pins of the OBC, similar to the bypasses. This will allow programming of the CubeSat OBC while the panels are attached. A [MOLEX 53261-1071](https://www.molex.com/molex/products/datasheet.jsp?part=active/0532611071_PCB_HEADERS.xml) is used for external connector, [MOLEX 53398-1071](https://www.molex.com/molex/products/datasheet.jsp?part=active/0533981071_PCB_HEADERS.xml&channel=Products&Lang=en-US) for the internal connector, and they are mounted on the –Z end of the panel. This connector is not required if the OBC will be left exposed during testing.

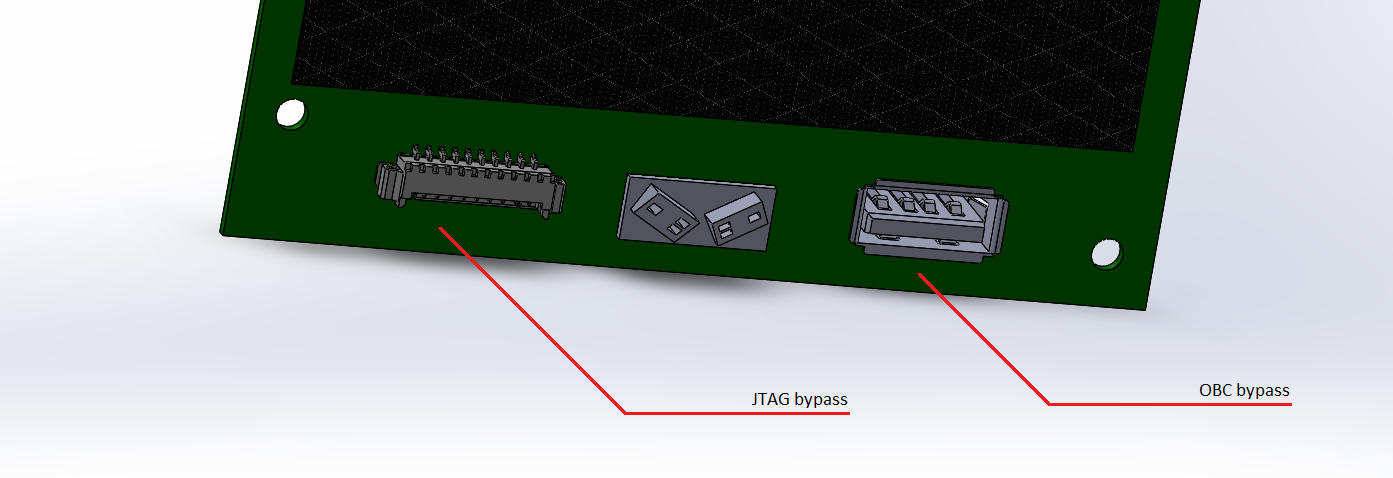


Figure 24, JTAG connector

# PCB design

The design of the PCB should fulfill several recommended requirements:

* The PCB material is FR4-Tg170.
* The PCB should have low outgassing properties (mainly material dependent).
* Two 70 µm internal copper layers (1st and 2nd layers) shall be embedded in the PCB.
  + These layers should be connected to the mounting holes.
* The PCB should be designed to the required shape (88.0mm x 215.0mm, with a 12.0mm x 14.0mm corner cut out according to the solar panel models).
* The PCB should have holes cut out for the various embedded connectors according to which panel face it is.
* The PCB should have all of the proper circuits and electrical connections made so that components and connectors may be mounted and connected properly.
* The PCB should have markings on the surface to help locate where to attach components.
* The electrical components (e.g. ADC, Op-Amps) should mounted on the bottom-side of the panel, with the exception of the photodiodes and temperature sensor.

The exact placement of components, solar cell solder points, etc. will be left to choice.

The site <https://www.4pcb.com/> may be used for producing prototypes and the final design of the PCB.

# Assembling the panels

All equipment, parts, and panel components should be on-hand, and electrical parts tested to reduce the chance of assembling a defective solar cell. The solar panel assembly process given here takes reference from the process used in reference [1], and refers to [2] for the bonding of additional silver foil connectors.



## Mounting of components

Care should be taken to follow all recommended practices with regards to attaching electrical components with regards to CSA guidelines.

1. Electrical testing of all components should be performed and ensure they meet the standards specified in their respective datasheets.
2. Examine the surface of the PCB for any defects in the panel surface.
3. Clean the PCB and ensure it is free of debris.
4. Insert any components that are to lie embedded in the PCB’s surface (USB connectors, RBF switch, etc.) and properly stake them to the PCB.
5. Mount the photodiode base and antenna release to the PCB.
6. Mount the appropriate electrical components to the PCB in their designated locations.
7. Mount the appropriate connectors on the top and bottom sides of the PCB.
8. Perform testing of all electrical components of the panel thus far (antenna release, sensors, bypasses, RBF switch, solar cell circuit), and ensure they are all working as intended.

## Preparing the solar cells

1. Inspect the solar cells for defects, cracks, stress marks etc. Set any such cells aside.
2. Ensure the interconnects are flattened.
3. Clean the cell and ensure it is free of debris.
4. Prepare a strip of silver foil.
5. Bond the strip to the designated location on the bottom-side of the cell (positive terminal) using silver epoxy. The strip should be exposed in the +Z direction of the solar cell.
6. Allow it to cure at 80°C for 3 hours.
7. Modify (cut or bend in a triangle shape) the connectors and silver foil to the appropriate lengths as required by the PCB solder points.



Figure 25, example of silver foil bonded with silver epoxy in [2]

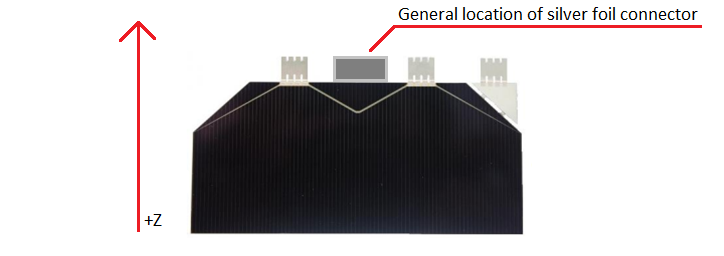


Figure 26, +Z direction and silver foil connector location

## Laying down solar cells

The application of the solar cells is the most important part of the process. **EXTREME CARE** must be taken when applying the cells, as once they are attached they may not be removed without damaging them. Additionally, the solar cells should be applied starting with the cell at the –Z end of the panel, and going in order to the +Z end of the panel. This is to avoid getting solder on a nearby, already attached solar cells, as the connectors are on the +Z side of the solar cell.

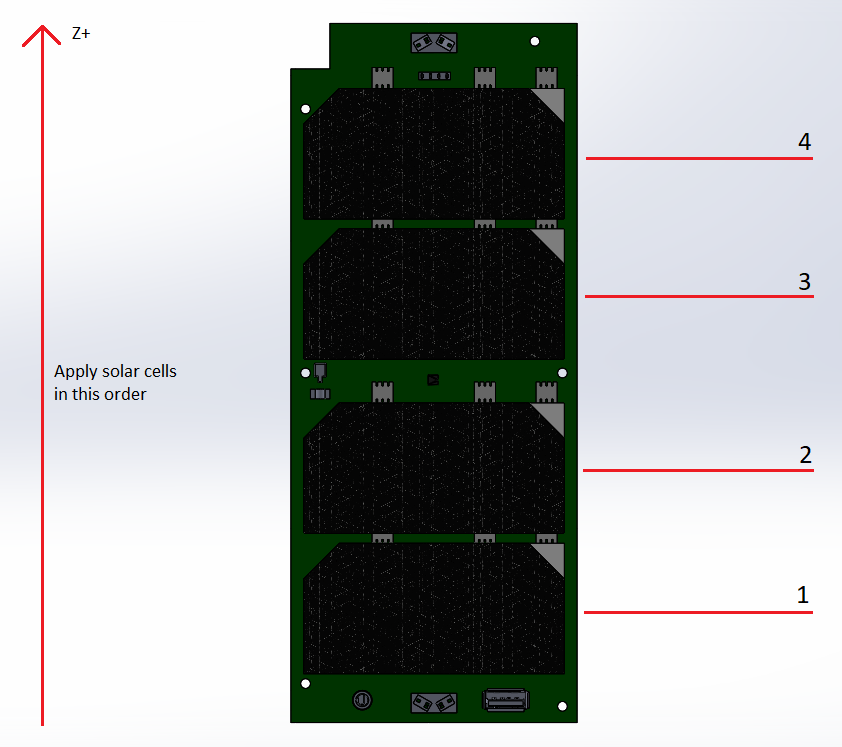


Figure 27, Solar cell application order

1. Place the solar cell template on the NuSil tape, and cut around the template with the Exacto blade. Ensure there are no tears. The cutout should cover the entirety of the area given by the template. The template should also allow for venting space around the silver foil connector on the bottom-side of the cell as shown in Figure 28.
2. Clean the surface of the PCB with solvent and flux remover to ensure there is no debris. Perform the final cleaning with isopropyl alcohol.
3. Place the cutout of the NuSil tape over the marked position for the solar cell on the PCB to verify that it covers the entire area.
4. Remove the covering on the NuSil tape that will be attached to the PCB.
5. Apply the NuSil tape by allowing one tip of the tape to contact the board, then slowly rolling the rest down. Apply pressure to ensure no air is trapped underneath.
6. Verify that the NuSil tape has been laid down properly. If not, remove it and clean the area, then repeat the application until correct.
7. Clean the bottom of the solar cell (positive terminal) with isopropyl alcohol and ensure no debris remains.
8. Remove the top covering of the NuSil tape to expose the adhesive.
9. Allow one tip of the solar cell to contact the adhesive, and slowly lay the cell down to avoid the trapping of air, while NOT applying pressure. Ensure that the cell is properly lined up before attempting, as it cannot be removed afterwards.
10. Starting at the end initially attached, use a credit card-like material to apply pressure and move towards the other side to attempt to remove any trapped air.
11. Inspect the bond to ensure it is complete and that there are no air bubbles present.
12. Trim any excess NuSil tape with the Exacto blade.
13. Repeat for the remainder of the solar cells.
14. Upon application of the final cell, perform testing to ensure the energy output of the solar panel meets the specified values.

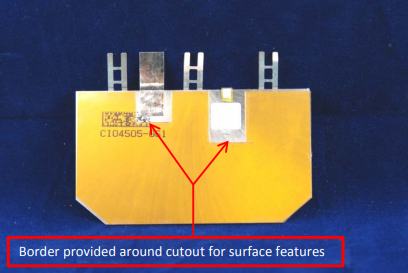


Figure 28, venting space around bottom-side components in [2]

# Environment and handling requirements

There are several environment requirements that should be followed during the assembly process of the solar cells.

## General

* The work area should be a class 100,000 or better cleanroom.
* The work areas should be grounded and non-static producing.
* The temperature of the environment should be regulated to acceptable component storage temperature requirements.
* Acceptable storage locations for components should be available.
* Glove wear should be used to prevent contamination of components.
* Soldering of components should be done according to their respective datasheets, e.g. taking into account maximum time a component may be at a certain temperature.
* The use of vacuum tweezers for handling is recommended.

## Solar cells

* The cell shall be protected from humidity and moisture, which may cause oxidation and corrosion of Ge substrate and other parts of the solar cell (metallization, III/V-semiconductor materials, antireflective coating ARC).
* The cells shall be transported and stored in dry conditions. Outgassing of any substances from the storage package has to be avoided.
* The recommended interface material for solar cell interconnectors is gold or silver.
* The soldering process of the solar cells requires the use of silver-saturated solder to avoid dissolution of the cell metallization. The soldering process temperature should not exceed 250°C for short time (about 1 min). The recommended solder material should be Sn96.5/Ag3.5 or any other suitable silver-saturated solder.
* Welding of interconnectors needs a specific set of parameter to avoid damage of epitaxial semiconductor stack.
* For solar cell cleaning purposes, ethanol or isopropyl alcohol are allowed at dimed light conditions. Different solvents in combination with light may induce voltage which could stimulate dendrite growth of the metallization with a certain risk of shunts.
* Shearing force to the metal finger grid shall be avoided.
* Smearing metal over the cell edge is not allowed due to risk of the short-circuit.
* At any process- and operation condition, solar cells shall be protected from electrical discharge (ESD).

Additional environment and handling requirements may be found in each component’s respective data sheets.

# Warnings and precautions

Several hazards are present when assembling solar cells, and precautions should be taken:

* GaAs on Ge solar cells contain harmful substances arsenic (As) and phosphorus (P) and shall be handled with care using appropriate hand protection (gloves). Handling tooling is necessary. Human consumption of cells, broken pieces and inhalation of dust may results in health problems and has to be avoided. In case of direct skin contact, hand washing is strongly recommended. In case of the cell breakage, cleaning up of contaminated parts is recommended.
* High temperatures are encountered during the soldering process, creating a risk of fire.
* Working with electrical components can create a risk of fire.
* Emergency equipment should be on hand (first aid, fire extinguishers, eye washes, etc.).

Additional warnings and precautions may be found in each component’s respective data sheets.

# References

[1] <http://citeseerx.ist.psu.edu/viewdoc/download?doi=10.1.1.386.7649&rep=rep1&type=pdf>

[2] <http://mstl.atl.calpoly.edu/~bklofas/Presentations/SummerWorkshop2009/Sat_1425_Solar%20Cell%20Installation%20Using%20Double%20Sided%20Polysiloxane%20PSA%20Film%20-%20Petras%20Karuza.pdf>

[3] <http://mstl.atl.calpoly.edu/~bklofas/Presentations/SummerWorkshop2017/SSC17-WK-50.pdf>

[4] PPD\_Coverage.m – MATLAB code used to find optimal coverage based on the facing normal vector of the photodiodes.

[5] Photodiode\_ADC.ino – Arduino code to read the digital output of the MAX1249 ADC with attached photodiodes.

[6] Specifications.xlsx – Excel file containing additional details on circuits, connector wiring, and a bill of materials.

[7] Testing\_results.docx – Document exploring the results of testing with the given components for the photodiodes sensor circuit.

[8] Photodiode\_angle\_analysis.docx – Document exploring the simulation to find the most optimal photodiode angle configuration for maximum coverage.